REMARKS

Claims 5-10, 18-21, and 23-37 are now pending in the application. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of this application.

ALLOWABLE SUBJECT MATTER.

Applicants thank the Examiner for indicating that claims 6, 8-10, 19, 30-32 and 34-35 are allowable if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants elect to defer rewriting of these allowable claims until the Examiner reviews the foregoing amendments and the following remarks.

CLAIM OBJECTION

The Office Action objected to claim 33 for containing several informalities. Claim 33 has been amended as suggested by the Examiner. In view of the foregoing amendments, Applicants believe that the objection to claim 33 is now moot, and thus, respectfully request the Examiner to reconsider and withdraw the instant objection.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(E)

A. Claim 18 is patentable over the art.

Claim 18 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,701,409 to Gates. Claim 18 recites:

> counting a number of external bus cycles that occur without onset of a new transaction on the external bus,
> determining [when] if the number meets a predetermined threshold,
> if so, generating a harassing transaction on the external bus.

Gates does not disclose, teach, or suggest these claimed features. First, Gates does not teach or suggest counting a number of external bus cycles without onset of a new transaction. Instead, Gates simply discloses waiting until a subsequent PCI bus cycle to post an error condition on the PCI bus. See Gates, col. 2, lines 43-46. Additionally, Gates' method is not conditional. Gates does not disclose generating a harassing transaction if the number of external bus cycles meets a predetermined threshold. Instead, Gates discloses posting *unconditionally* an error condition onto the PCI bus during a subsequent bus cycle. Thus, Gates fails to disclose, teach, or suggest either counting the number of external bus cycles or

determining whether the number of external bus cycles meets a predetermined threshold. Accordingly, claim 18 is patentable over the cited art.

B. Claims 20-21 and 23 are patentable over the art.

Claim 20 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,609,221 to Coyle et al. Amended claim 20 recites in part:

> the validation FUB further comprising: . . .
> a request library in communication with the transaction latch and having an output coupled to the data request pipeline, and to store transaction request types according to an external bus protocol.

Coyle does not teach or suggest the claimed features as defined in claim 20. In paragraph 23, the Office Action alleges that a pattern storage disclosed in Coyle is equivalent to the request library of claim 20. Applicants respectfully disagree. Coyle's pattern storage simply holds one or more testing patterns. Among these patterns that are stored in the pattern storage, Coyle's pattern source selects a pattern that is to be used as a stimulus cycle. Coyle's pattern source, however, does not store transaction request types according to an external bus protocol. For at least these reasons, independent claim 20 is patentable over the cited art. Claims 21 and 23, which depend from independent claim 20, are also patentable over the art.

C. Claims 29 and 33 are patentable over the art.

Claims 29 and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Coyle. Claim 29 recites in part:

> reading an address of the first transaction from the external bus, and
> in response to the detected transaction, issuing a read request in a second transaction on the external bus, the read request directed to the same address as the first transaction.

Claim 33 recites in part:

> detecting a plurality of transactions posted on an external bus if a predetermined condition is met,
> reading addresses of the transactions.

Coyle does not teach, or suggest the claimed features of claims 29 and 33. The Office Action alleges that claims 29 and 33 are anticipated because Coyle discloses generating a replica [of a testing pattern] and send it [to a second device] over the bus. Applicants respectfully disagree.

Coyle discloses a loop-back testing method in which a second device receives a testing pattern (a stimulus cycle) from a first device and simply echoes the pattern back to the first

device. Neither the first device nor the second device reads an *address* of the testing pattern. In fact, Coyle's first and second devices do not even attempt to extract any type of information from the testing pattern transmitted between the two devices.

Additionally, Coyle does not disclose issuing a read request in a second transaction on the external bus, where the read request is directed to the same address as the first transaction. Coyle does not describe the nature of his test patterns, other than to describe them as data. Coyle nowhere relates the data pattern to any bus protocol. He certainly does not describe any test pattern as being read requests, much less the second transaction on the external bus.

Moreover, Coyle does not disclose, teach, or suggest detecting a plurality of transactions posted on an external bus if a predetermined condition is met. Coyle's method is not conditional. Coyle's second device receives the entire testing pattern, and echoes the entire testing pattern back to the first device.

For at least these reasons, independent claims 29 and 33 are patentable over the cited art.

In view of the foregoing, reconsideration and withdrawal of the §102 rejection is respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103(A)

A. Claims 5, 7, and 36-37 are patentable over the art.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being obvious over Coyle in view of U.S. Patent No. 5,142,673 to De Angelis et al. Claim 5 recites:

> if a request type of the transaction matches a triggering condition,
> generating a data request, and
> generating a harassing bus transaction based on the data request.

Likewise, claim 36 recites in part:

> storing a request type in a register,
> when the request type of the external bus transaction matches the request type stored in the register, generating a data request on the external bus.

Coyle, either alone or in view of De Angelis, does not disclose, teach, or suggest these claimed features. In particular, Coyle does not relate his data patterns to any bus protocol. Coyle does

not describe anything about the request type of his testing patterns. Additionally, Coyle also fails to disclose generating a data request under any circumstances or generating a harassing bus transaction based on the data request.

De Angelis does not cure Coyle's deficiency. De Angelis discloses a bus monitoring device that uses a trigger memory to selectively detect and record trigger conditions at selected points within a system. De Angelis' device includes a trigger generating means, which generates a pattern of trigger signals for each trigger condition at one of the selected points. De Angelis, however, also describes nothing about the request type of his trigger signals. Moreover, De Angelis does not generate a harassing bus transaction based on the data request. Thus, Coyle, either alone or in combination with De Angelis, fails to disclose, teach, or suggest the claimed subject matter as defined in claims 5 and 36 For at least these reasons, independent claims 5 and 36 are patentable over the cited art. Claims 7 and 37, which depend from claims 5 and 36, respectively, are also patentable over the art.

B. Claims 24-28 are patentable over the art.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being obvious over Coyle in view of De Angelis. Claim 27 stands rejected under 35 U.S.C. § 103(a) as being obvious over Coyle in view of De Angelis and U.S. Patent No. 5,151,981 to Westcott et al. Claims 24 and 27 recite in part:

> a processor core;
> a bus sequencing unit in communication with the processor core and an external bus, the bus sequencing unit further comprising an arbiter, a cache memory, and a transaction queue; and
> a validation FUB in communication with the bus sequencing unit and the external bus.

The Office Action alleges that Coyle's testing logic is equivalent to both the validation FUB and the bus sequencing unit of claims 24 and 27. In particular, the Office Action alleges that Coyle discloses a bus sequencing unit having an arbiter to receive a data request because Coyle's testing logic arbitrates the normal circuitry to assume control of the bus for testing purposes using a switch 422. Applicants respectfully disagree. Coyle simply switches between its normal mode and diagnostic mode using the switch 422. This implies that Coyle's testing logic becomes functional only during its diagnostic mode. Moreover, Coyle does not disclose his testing patterns being bus protocols. Thus, Coyle says nothing about either a bus

sequencing unit or an arbiter to receive a data request. Accordingly, Coyle fails to teach a bus sequencing unit having an arbiter to receive a data request.

De Angelis and/or Westcott do not overcome Coyle's deficiency. As mentioned above, De Angelis discloses a bus monitoring device having a trigger generating means, which generates triggering signals for each triggering condition at one of the selected points. De Angelis, however, says nothing about a bus sequencing unit having an arbiter to receive a data request.

Westcott discloses a system for executing instructions out-of-sequence. Westcott, however, also fails to disclose a bus sequencing unit having an arbiter to receive a data request.

Thus, Coyle, either alone or in combination with De Angelis and/or Westcott, fails to disclose, teach, or suggest the claimed features as defined in claims 24 and 27. For at least these reasons, independent claims 24 and 27 are patentable over the cited art. Claims 25-26 and 28, which depend from claims 24 and 27, respectively, are also patentable over the art.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 103(a) rejections.

CONCLUSION

All claims are allowable over the cited art. Applicants respectfully request allowance of the application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Kenyon & Kenyon Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at (202) 220-4235 to discuss any matter concerning this application.

Respectfully submitted,

Date: 7/02/04

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